VERIFICATION OF TRANSLATION

I, YABUTA Kimikazu, a citizen of Japan, currently residing at 4-3-2 Kizuri HIgashiosaka, Osaka, Japan, hereby declare:

That I am fully familiar with the English language and with the Japanese language in which the accompanying Japanese patent applications No. 117445/1988 and 161665/1995 were prepared;

That the annexed English text is believed by me to be a true and accurate translation of the text of said Japanese patent applications; and

That all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed at Osaka, Japan

Date: May 7, 2003

Signature: Yabuta Kimikazu

YABUTA Kimikazu

Japanese Laid-Open Patent Application No. 161665/1995 (Tokukaihei 7-161665) (Published on June 23, 1995)

(A) Relevance to claim

The following is a translation of passages related to claim 1 of the present invention.

(B) Translation of the relevant passages

[EMBODIMENTS]

(Embodiment 1) Fig. 1 is an explanatory drawing that shows processes of the present invention; and Fig. 1(a) shows a process for forming a protective film, Fig. 1(b) shows a process for cutting a semiconductor wafer, Fig. 1(c) shows a process for etching the cut face of a chip, and Fig. 1(d) shows a process for removing the protective film. Fig. 2 is a schematic view that shows the structure of a dicing device, and Fig. 3 is a plan view that shows the surface of a semiconductor wafer that is to be cut.

[0010] (Process for forming a protective layer) Novolak resin is dropped onto the surface of the semiconductor wafer 1 so that this is rotated within the horizontal face so as to form a protective layer 2. The resin is used for protecting the semiconductor device circuit, and is transparent so as to allow confirmation of lines that indicate a dicing area.

[0011] (Process for cutting a semiconductor wafer) As illustrated in Fig. 2, a dicing blade 12 is provided as a cutting means for cutting the semiconductor wafer 1, and a wafer fixing table 13 is provided as a wafer fixing means for securing the semiconductor wafer 1. The dicing blade 12 is attached to the main shaft 16 of a main shaft head 15 that is supported by a supporting column 14. The supporting column 14 is vertically secured to a head 17 having a fixed structure, and the main shaft head 15 is allowed to move up and down in the vertical direction along the supporting column 14. Here, the main shaft 16 extends in the horizontal direction, and is rotated at a high speed.

[0012] Here, the wafer fixing table 13, which is attached to the upper surface of the head 17, is allowed to move straight along two axes that are orthogonal to each other in horizontal directions. Moreover, the upper surface of the wafer fixing table 13 forms a horizontal wafer securing face 18 so that the face 18 is allowed to rotate in forward and reverse directions centered on an axis line in the vertical direction. The semiconductor wafer 1 is secured onto the wafer securing face 18 by means of vacuum suction, preferably in a state where it is affixed to the dicing tape 19.

[0013] Moreover, the dicing device 10 of the present

9-15/665

embodiment is provided with a CCD camera 20 that is an image pick-up means for picking up an image of the surface of the semiconductor wafer 1, at a lower portion of the main shaft head 16. The CCD camera 20 is capable of picking up an image of an area adjacent to the dicing blade 12. Here, the CCD camera 20 is connected to a computer 22 serving as an image-processing means through an A/D converter 21. Analog information of an image, picked up by the CCD camera 20, is digitized by the A/D converter 21, and then inputted to the computer 22. The computer 22 carries out an image-processing operation on the inputted image information in accordance with a suitable algorithm so that the position of a cut line can be detected. The positional information of the cut line detected by the computer 22 is inputted to a controller (control means) 23 that controls the rotation of the dicing blade 12, the up and down movements of the main shaft head 15 and the movement in the horizontal direction of the wafer securing table 13; thus, the semiconductor wafer 1 is cut along the corresponding cut line. With this device, the semiconductor wafer 1, controlled by the controller 23, is automatically cut along the center line of a scribe line S, and divided into a plurality of chips 3.

[0014] (Process for chemically etching the cut face of a

7-161666

chip) When a semiconductor wafer is cut by the dicing blade, fine irregularities occur on the cut face 3-1, and machining distortions also occur thereon. Upon dicer test, cracks occur from these irregularities, and these cracks are developed by the machining distortions. Therefore, the chip 3 after the dicing process is immersed in an etchant 4 so that the machining-affected layer is removed so as to form a smooth surface.

[0015] With respect to the etchant, a sulfuric-acid-based solution (H_2SO_4 + H_2O + H_2O) or an ammonia-based solution (NH_4OH + H_2O_2 + H_2O) is preferably used. Upon application of these solutions, the etching rate is virtually set to 1 μm/min, in which the affected layer can be removed in five minutes.

[0016] (Process for removing a protective film) The chip 3, cut as described above, is immersed in a solvent 5 such as acetone, and washed so that the protective film 2, which serves as resist, is removed.

[0017] In accordance with the above-mentioned processes, a wafer, made of GaAs, having a diameter of 3 inches is cut so as to form chips of 2 mm × 2 mm. These chips were secured onto a substrate with a bonding agent, and this was subjected to a shearing test. As a result, any of these chips were separated at a load of 8 kg, thereby indicating stable shearing strength. In contrast, the

7-161665

same test was carried out on chips that had not been subjected to etching after the dicing process, and many of these had cracks at a shearing force of 4 to 5 kg.

7-181665.

Japanese Laid-Open Patent Application No. 117445/1988 (Tokukashou 63-117445) (Published on May 21, 1988)

(A) Relevance to claim

The following is a translation of passages related to claim 1 of the present invention.

(B) Translation of the relevant passages

[EMBODIMENTS]

Referring to Figures, the following description will discuss embodiments of the present invention.

Referring to Fig. 1, an explanation will be given of the first embodiment of the present invention. Fig. 1, which shows processes for carrying out a machining method of a semiconductor wafer in accordance with the first embodiment of the present invention, includes schematic cross-sectional views of the semiconductor wafer in the respective processes.

Additionally, in the first embodiment and a second embodiment (which will be discussed later), processes taken until completion of the IC formation are the same as those conventionally used.

a) Completion of IC formation

b) Bumping process

Bumps are formed on an IC by electrolytic plating.

c) Dicing process

Grooves are formed from the surface of an IC wafer 1 up to a predetermined depth along IC chips.

d) Wax applying process

Wax 3 is applied so as to protect the surface of the IC wafer 1 from an etchant 4.

e) Etching process

The semiconductor wafer 1 is immersed into the etchant 4 so that the surface of the semiconductor wafer 1 is subjected to an etching process until it has reached a predetermined width.

Moreover, although not shown in Fig. 1, upon completion of the etching, the semiconductor wafer 1 is washed with water so as to remove the etchant 4 therefrom.

Furthermore, the semiconductor wafer 1 is washed with a solvent so as to remove the wax from the surface thereof.

f) Breaking process

The semiconductor wafer 1 is subjected to a breaking process so as to be separated into IC chips 5.

In the above-mentioned embodiment, in order to protect the surface of the semiconductor wafer 1, the wax 3 needs to be made of a material which is resistant to the etchant 4, gives no adverse effects to the element area of the semiconductor wafer 1, and is readily washed by a

63-117445

specific solvent. With respect to such a wax material, fluororesins, etc. are preferably used.

Moreover, it is necessary for the etchant 4 to have a stable etching rate to the semiconductor wafer 1, and to be less susceptible to variations in the amount of etching inside the semiconductor wafer 1. With respect to such an etchant, for example, in the case when silicon is used as a material of the semiconductor wafer 1, hydrofluoric acid, nitric acid, a mixed acid of acetic acid, etc. are preferably used.

Next, referring to Fig. 2, the following description will discuss the second embodiment of the present invention. In the same manner as Fig. 1, Fig. 2 shows processes for carrying out a machining method of a semiconductor wafer in accordance with the embodiment of the present invention, and includes schematic cross-sectional views of the semiconductor wafer in the respective processes.

Processes from a) to b) are the same as those of the first embodiment; therefore, the description thereof is omitted.

c) Dicing process

A semiconductor wafer 1 is subjected to a dicing process up to a predetermined remaining thickness. In this case, the remaining thickness 6 from dicing is

63-117445

smaller than the thickness etched.

d) Wax applying process

The semiconductor wafer 1 is fixed to a supporting substrate 7 with wax 3 which provides protection to the surface of the semiconductor wafer 1 and adhesion to the supporting substrate 7.

e) Etching process

The semiconductor wafer 1, together with the supporting substrate 7, is dipped in an etchant 4 to subject the surface to etching until the semiconductor wafer 1 has a predetermined thickness.

The remaining thickness 6 from dicing is smaller than the thickness etched; therefore, when the etching process is complete, the semiconductor wafer 1 is separated into IC chips 5, but remains fixed to the supporting substrate 7.

Then, although not shown in Figure 2, after the etching process is complete, the semiconductor wafer 1 together with the supporting substrate 7 is washed in water to get rid of the etchant 4.

f) Wax washing process

The semiconductor wafer 1 together with the supporting substrate is washed in a solvent. Upon etching down to a predetermined thickness, the semiconductor wafer 1 is already separated into the IC chips 5; the

63-117445

smaller than the thickness etched.

d) Wax applying process

The semiconductor wafer 1 is fixed to a supporting substrate 7 with wax 3 which provides protection to the surface of the semiconductor wafer 1 and adhesion to the supporting substrate 7.

e) Etching process

The semiconductor wafer 1, together with the supporting substrate 7, is dipped in an etchant 4 to subject the surface to etching until the semiconductor wafer 1 has a predetermined thickness.

The remaining thickness 6 from dicing is smaller than the thickness etched; therefore, when the etching process is complete, the semiconductor wafer 1 is separated into IC chips 5, but remains fixed to the supporting substrate 7.

Then, although not shown in Figure 2, after the etching process is complete, the semiconductor wafer 1 together with the supporting substrate 7 is washed in water to get rid of the etchant 4.

f] Wax washing process

The semiconductor wafer 1 together with the supporting substrate is washed in a solvent. Upon etching down to a predetermined thickness, the semiconductor wafer 1 is already separated into the IC chips 5; the

63-117445

individual IC chips 5 are obtained by washing the wax 3 forming the bonding layer, without the need for breaking.

In the second embodiment, the etching process to the rear face of the semiconductor wafer 1 and the separation process into the IC chips 5 can be carried out in one process, and another advantage is that a smooth cut face is obtained without cracks and protrusions due to cleavage of monocrystal on the side face of the IC chip 5.

63-117445